

**NCC 1T 8051-MCU**

**ATM8F8040A**

**Datasheet**



目录

**1. Core Features ..... 3**

**2. Description .....4**

**3. Block diagram .....5**

**4. Pins description and alternate functions .....6**

**5. Package information ..... 9**

    5.1. TSSOP20 ..... 9

    5.2. QFN20 ..... 10

    5.3. SOP16 .....11

**6. Electrical characteristics .....12**

    6.1. Limit parameters ..... 12

    6.2. DC Characteristics ..... 12

    6.3. ADC Characteristics ..... 13

    6.4. IHRC Characteristics ..... 13

    6.5. ILRC Characteristics ..... 14

    6.6. CRY Characteristics ..... 14

    6.7. Flash memory Characteristics ..... 14

    6.8. NRST and EXTI Characteristics ..... 14

    6.9. EFT Characteristics ..... 14

    6.10. ESD Characteristics ..... 14

    6.11. Latch up Characteristics ..... 15

**7. Chip type ..... 16**

**8. Revision history ..... 17**

## 1. Core Features

### CPU

8-bit 1T 8051 core  
 1/2/4/8 System Clock Division  
 Dual DPTR  
 Dual-line debugging

### ROM

16K bytes FLASH Program Memory(1K erase/write cycles)  
 128 bytes EEPROM(10K erase/write cycles) data retention: 10 years

### RAM

256 bytes IRAM  
 512 bytes XRAM

### GPIO

Up to 18 I/O pins  
 Interrupt on any port change

### Timer/PWM

16-bit 8051 standard timers T0/T1  
 16-bit timer T2 with capture and programmable output  
 16-bit pwm with 7-channels complementary outputs

AWU

WDT

### Others

CRC16 calculation unit  
 Configurable logic cell (CPL)  
 External crystal oscillator stop detection

### Communication

two UARTs

### Analog Peripherals

12-bit and 10 channels ADC  
 Power-on reset  
 Brownout reset

### Clock management

Internal 32MHz RC( $\pm 1\%$ )  
 Internal 32KHz RC  
 1 to 20MHz crystal oscillator

### Mode

Normal mode  
 IDLE mode  
 STOP mode, minimum current  $< 1\mu\text{A}$

### Operating Characteristics

Clock: up to 32MHz  
 Voltage Range: 2.7~5.5V  
 Temperature Range:  $-40^{\circ}\text{C}\sim 85^{\circ}\text{C}$

### Package

TSSOP20  
 QFN20  
 SOP16

## 2. Description

ATM8F8040A is an 8-bit MCU with 16K bytes of Flash program memory. It has the following features: 16K bytes of Flash program memory, 256 bytes of SRAM, 512 bytes of extended XRAM, 128 bytes of internal EEPROM, two 16-bit high-performance timers T0/T1, one 16-bit timer T2 with 3-channels capture, one PWM with dead-time, one WDT, two UARTs, one 12-bit ADC, one CRC, one configurable logic cell (CPL). ATM8F8040A suitable for consumer and control electronic product applications.



3. Block diagram

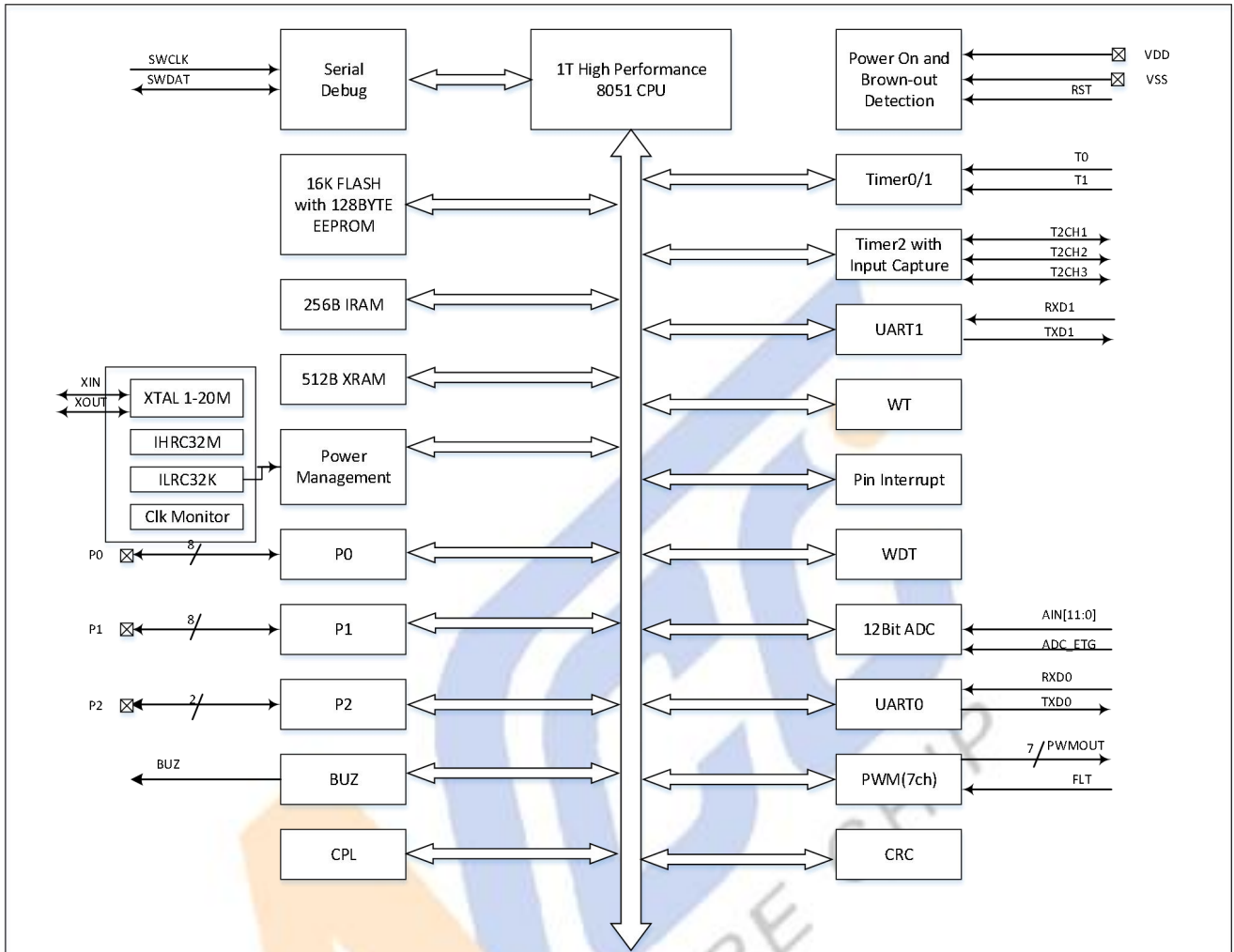


Figure 3-1 Block diagram

**4. Pins description and alternate functions**

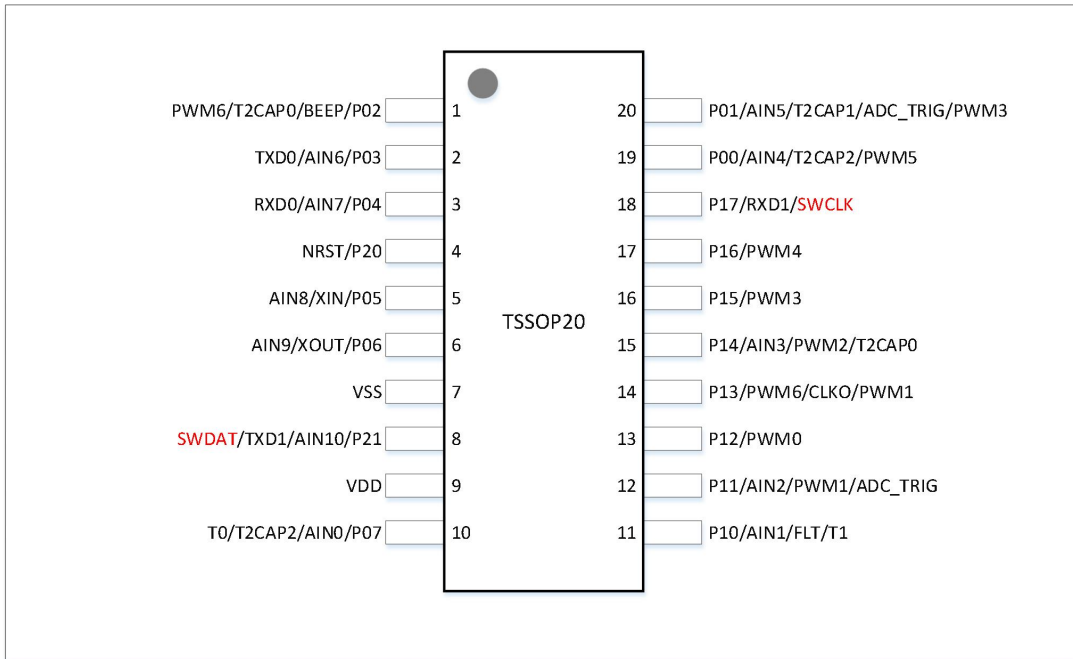
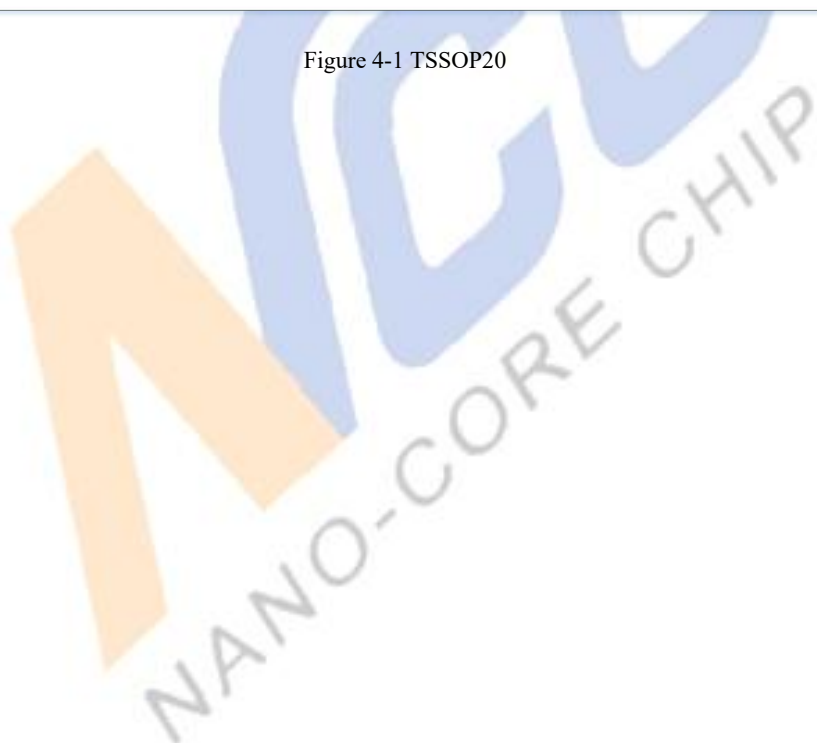


Figure 4-1 TSSOP20



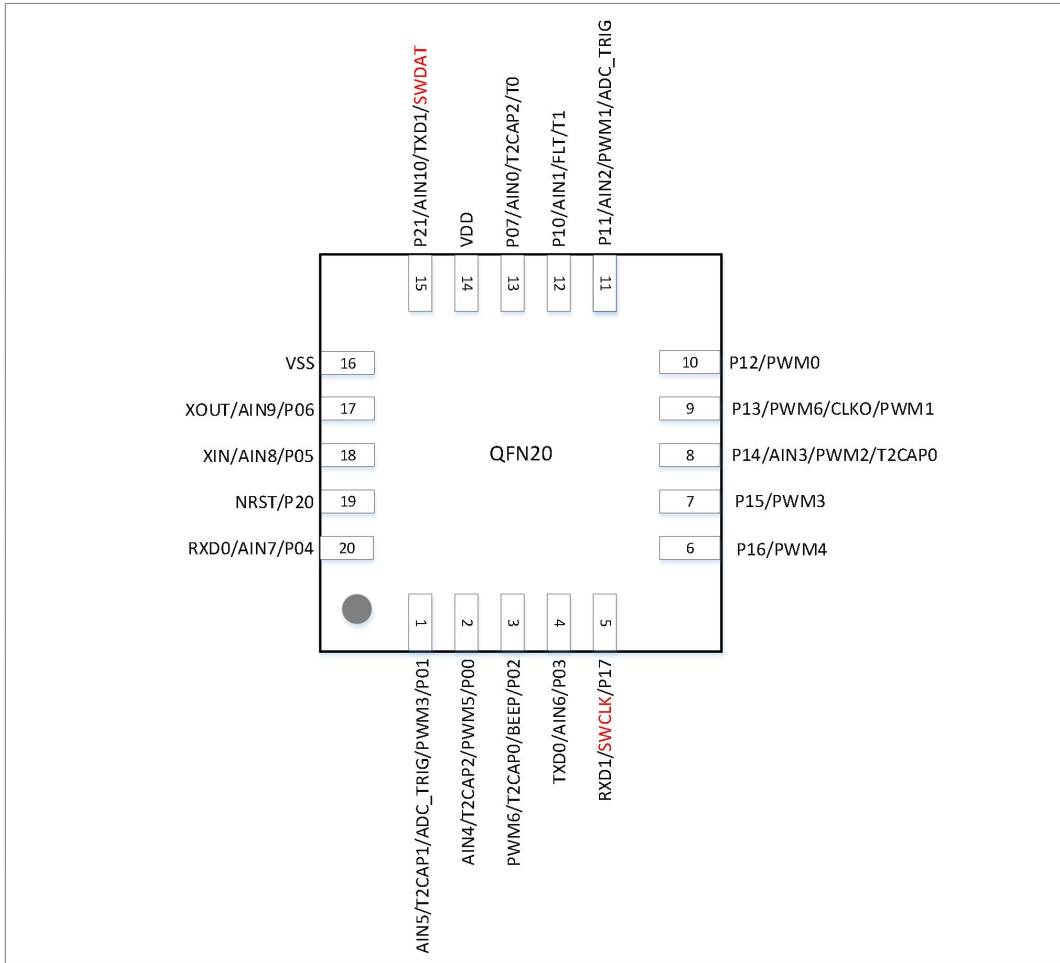


Figure 4-2 QFN20

NANO-CORE CHIP

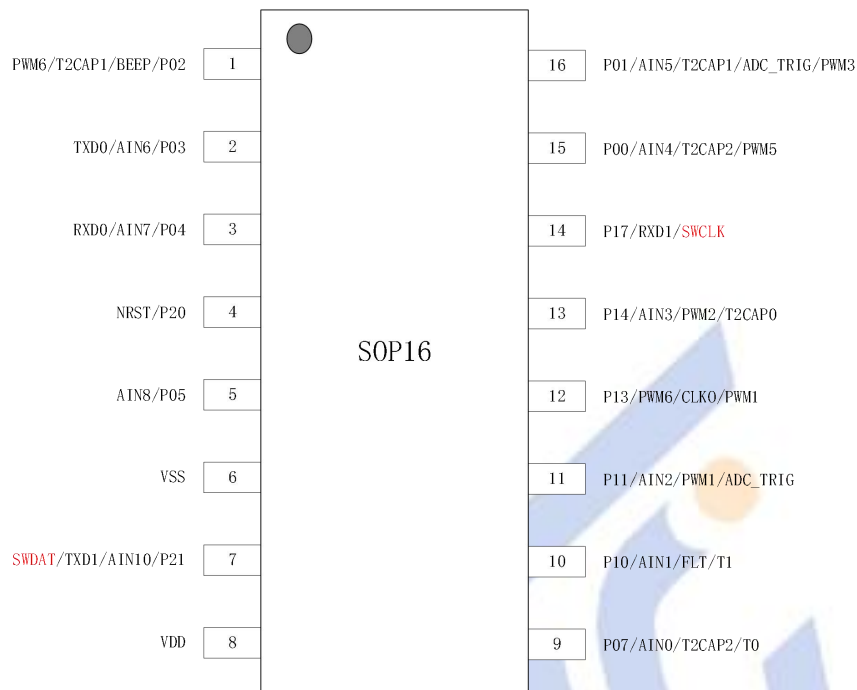


Figure 4-3 SOP16

Table 4- 1 Pins description

TSSOP20	QFN20	SOP16	I/O	Alternate Functions
1	3	1	P02	PWM6/T2CAP0/BEEP
2	4	2	P03	TXD0/AIN6
3	20	3	P04	RXD0/AIN7
4	19	4	P20	NRST
5	18	5	P05	AIN8/XIN
6	17		P06	AIN9/XOUT
7	16	6	VSS	
8	15	7	P21	SWDAT/TXD1/AIN10
9	14	8	VDD	
10	13	9	P07	AIN0/T2CAP2/T0
11	12	10	P10	AIN1/FLT/T1
12	11	11	P11	AIN2/PWM1/ADC_TRIG
13	10		P12	PWM0
14	9	12	P13	PWM6/CLK0/PWM1
15	8	13	P14	AIN3/PWM2/T2CAP0
16	7		P15	PWM3
17	6		P16	PWM4
18	5	14	P17	SWCLK/RXD1
19	2	15	P00	AIN4/T2CAP2/PWM5
20	1	16	P01	AIN5/T2CAP1/ADC_TRIG/PWM3



**5. Package information**

5. 1. TSSOP20

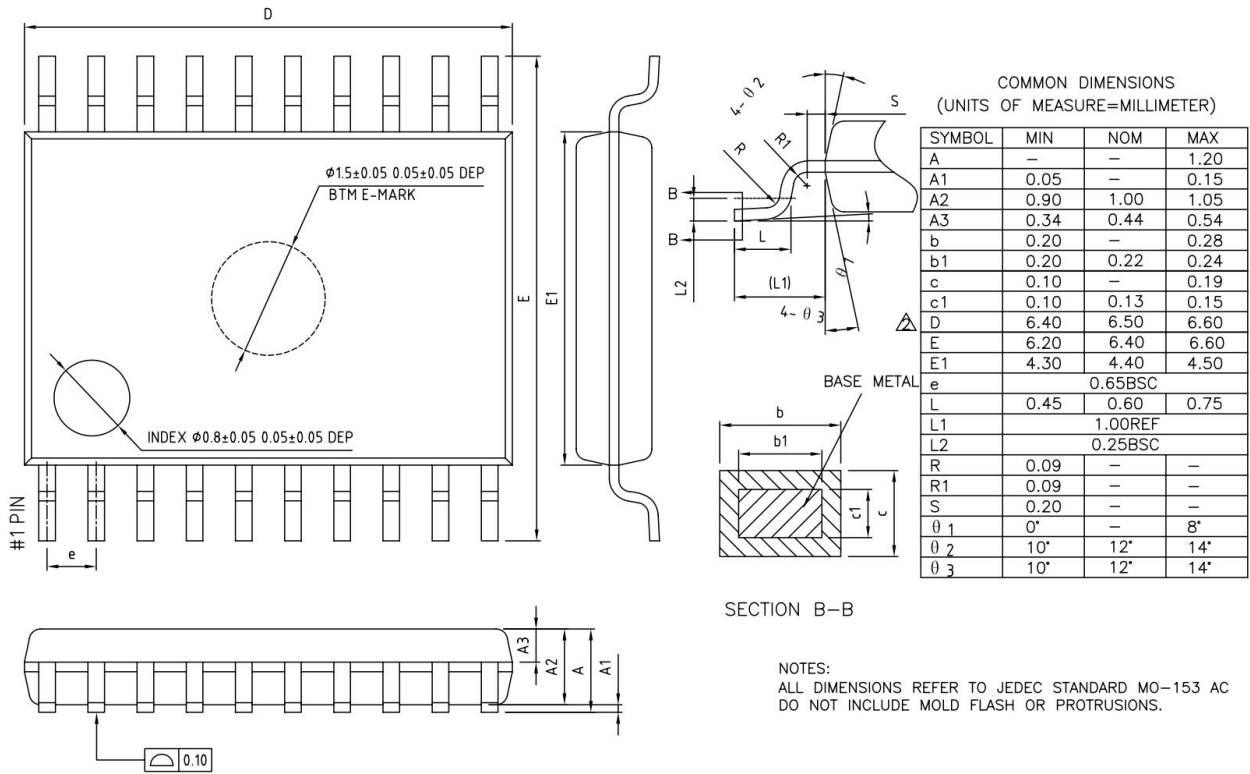
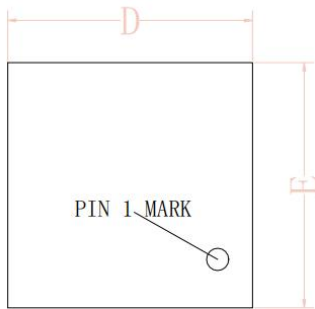


Figure 5-1 TSSOP20 package information

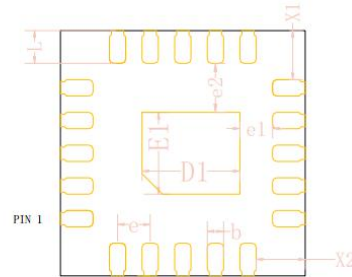


5. 2. QFN20

Package Top View



Package Bottom View



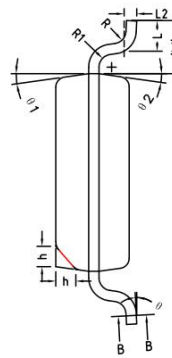
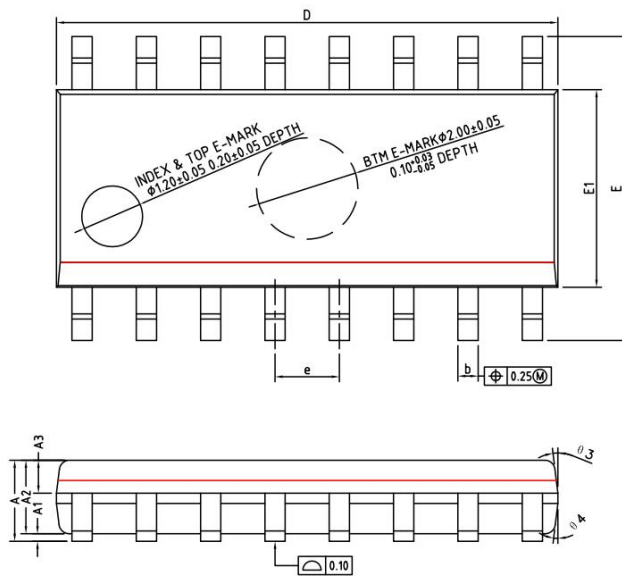
Package Side View



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	1.150	1.200	1.250
E1	0.950	1.000	1.050
L	0.350	0.400	0.450
b	0.150	0.200	0.250
e	0.350	0.400	0.450
e1	0.350	0.400	0.450
e2	0.550	0.600	0.650
X1	0.550	0.600	0.650
X2	0.550	0.600	0.650

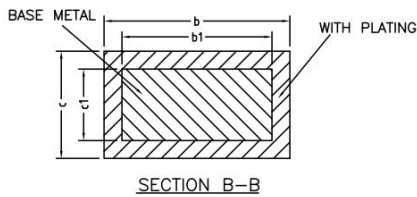
Figure 5-2 QFN20 package information

5.3. SOP16



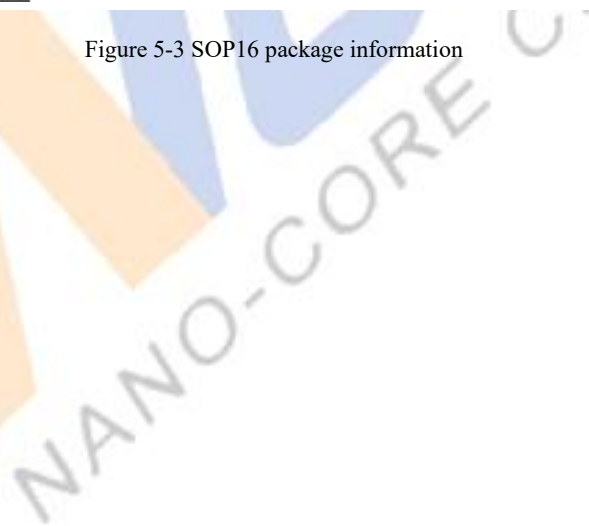
COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.55	0.65	0.75
b	0.36	—	0.51
b1	0.35	0.40	0.45
c	0.18	—	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.22	1.27	1.32
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	—	—
R1	0.07	—	—
h	0.30	0.40	0.50
θ	0°	—	8°
θ 1	6°	8°	10°
θ 2	6°	8°	10°
θ 3	5°	7°	9°
θ 4	5°	7°	9°



NOTES:  
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC  
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 5-3 SOP16 package information



## 6. Electrical characteristics

### 6.1. Limit parameters

Table 6-1 limit parameters

Symbol	Parameters	Range	Unit	Others
VDD	External supply voltage	-0.3~6.0	V	-
T <sub>STG</sub>	Storage temperature range	-40~125	°C	-
T <sub>opt</sub>	Operating temperature	-40~85	°C	-
V <sub>I</sub>	Input voltage on I/O	-0.3~VDD+0.3	V	-
V <sub>O</sub>	Output voltage on I/O	-0.3~VDD+0.3	V	-
I <sub>OLT</sub>	Total current sunk by sum all I/Os	100	mA	Max
I <sub>OHT</sub>	Total current sourced by sum of all I/Os	-100	mA	Max

### 6.2. DC Characteristics

Table 6-2 Voltage and Current characteristics

If there are no other instructions, VDD-VSS=5V, TA=25°C

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Operating Voltage	F <sub>HRC</sub> =32MHz, F <sub>CPU</sub> =8MHz <sup>[1]</sup>	4.5		5.5	V
		F <sub>HRC</sub> =16MHz, F <sub>CPU</sub> =4MHz	2.7		5.5	V
I <sub>DD1</sub>	Operating Current	F <sub>System</sub> =32MHz;F <sub>CPU</sub> =8MHz;ADC disabled;all I/Os push-pull output without load;P1 toggled;		12.5		mA
I <sub>DD11</sub>	Operating Current	F <sub>System</sub> =16MHz;F <sub>CPU</sub> =4MHz;ADC disabled;all I/Os push-pull output without load;P1 toggled;		7.5		mA
I <sub>DD2</sub>	IDLE Current(IDLE)	F <sub>System</sub> =4MHz;F <sub>CPU</sub> =2MHz;ADC disabled;All peripherals disabled;CPU is idle		1.9		mA
I <sub>DD3</sub>	IDLE Current(STOP)	All analog peripherals disabled;BOR enable;CPU is stop		40		uA
I <sub>DD4</sub>	IDLE Current(STOP)	All analog peripherals disabled;Internal LRC enable;WT enable;CPU is stop		3		uA
I <sub>DD5</sub>	IDLE Current(STOP)	All analog disabled;BOR disable;CPU is stop		1		uA
V <sub>IH1</sub>	I/O input high level voltage		0.7			VDD
V <sub>IL1</sub>	I/O input low level voltage				0.3	VDD
I <sub>IL</sub>	leakage current	Input low level voltage			1	uA
I <sub>IH</sub>	leakage current	Input high level voltage			1	uA
V <sub>OH</sub>	Output high level voltage	I <sub>src</sub> =10mA	0.9			VDD
V <sub>OL1</sub>	Output low level voltage (except P11/P12/P13/P14/P15/P16/P00/P01)	I <sub>sink</sub> =20mA			0.1	VDD
V <sub>OL2</sub>	Output low level voltage	I <sub>sink</sub> =50mA			0.2	VDD

	(P11/P12/P13/P14/P15/ P16/P00/P01)					
R <sub>PUL1</sub>	Pull-up (except P20)			50		KΩ
R <sub>PUL2</sub>	Pull-up(P20)			150		KΩ
BOR	Brownout reset threshold	BOR level=4.3V	4.2	4.3	4.4	V
		BOR level=3.7V	3.6	3.7	3.8	V
		BOR level=2.9V	2.8	2.9	3.0	V
		BOR level=2.5V	2.4	2.5	2.6	V

[1]Internal HRC is configured by tool. CPU clock is configured by system clock division and FLASH wait time PWAIT.

### 6.3. ADC Characteristics

Table 6-3 ADC Characteristics  
(TA=25°C)

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Supply voltage	VDD=5V	2.7		5.5	V
V <sub>IREF1</sub>	Internal reference voltage	VDD=5V	1.94	2.0	2.06	V
V <sub>IREF2</sub>		VDD=5V	2.34	2.4	2.46	V
V <sub>IREF3</sub>		VDD=5V	3.54	3.6	3.66	V
V <sub>EREF</sub>	External reference voltage	VDD=5V			VDD	
V <sub>IN</sub>	Conversion voltage range	VDD=5V	0		VREF	V
N <sub>R</sub>	Accuracy	VDD=5V		12		Bit
DNL	Differential non linearity	VDD=5V			2	LSB
INL	Integral non linearity	VDD=5V			±3	LSB
E <sub>F</sub> <sup>[1]</sup>	Gain error	VDD=5V			±4	LSB
E <sub>AD</sub> <sup>[1]</sup>	Total absolute error	VDD=5V			±8	LSB
E <sub>Z</sub> <sup>[1]</sup>	Offset error	VDD=5V			±4	LSB
F <sub>ADC1</sub>	Clock frequency	4.5~5.5V			2	MHz
F <sub>ADC2</sub>		2.7~5.5V			1	MHz
T <sub>ADC</sub>	Conversion time	VDD=5V		13.5		TCK
T <sub>SAMP1</sub>	Sampling time	VDD=5V,F <sub>ADC</sub> =2MHz	4		16	TCK
T <sub>SAMP1</sub>		VDD=3V,F <sub>ADC</sub> =1MHz	4		16	TCK
C <sub>ADC</sub>	CADC <sup>[2]</sup>	VDD=5V		25		pF

[1] The value is calibrated by software

[2] Guaranteed by design

### 6.4. IHRC Characteristics

Table 6-4 IHRC Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Operating voltage		2.7		5.5	V
F <sub>req</sub>	Frequency	Calibration value		32		MHz
F <sub>var</sub>	Frequency error	25°C,5V	-1		+1	%
		-40 ~ +85°C ,2.7V~5.5V	-3		+3	%

## 6. 5. ILRC Characteristics

Table 6- 5 ILRC Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Operating voltage		2.7		5.5	V
F <sub>req3</sub>	Frequency	Calibration value		32		kHz
F <sub>var2</sub>	Frequency error	-40 ~ +85°C ,2.7V~5.5V	-10		+10	%

## 6. 6. CRY Characteristics

Table 6- 6 CRY Characteristics

(TA=25°C, 2.7V~5.5V)

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
F <sub>req</sub>	Frequency	4.5V<VDD<5.5V,CL=22pF	1.0		20.0	MHz
		3.0V<VDD<5.5V,CL=30pF	1.0		12	MHz
		2.7V<VDD<5.5V,CL=30pF	1.0		8	MHz

## 6. 7. Flash memory Characteristics

Table 6- 7 FLASH memory Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Operating voltage	-40 ~ +85°C	2.7 <sup>[1]</sup>		5.5	V
V <sub>DDR</sub>	Operating temperature	read and write,VDD=5V	-40		85	°C

[1]The minimum voltage for flash write is 4.5v

Table 6- 8 EEPROM Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
V <sub>DD</sub>	Operating temperature	-40°C~+125°C	2.7		5.5	V
V <sub>DDR</sub>	Operating temperature	read and write,VDD=5V	-40		85	°C

## 6. 8. NRST and EXTI Characteristics

Table 6-9 NRST and EXTI Characteristics

(TA=25°C, 5V)

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
T <sub>INT</sub>	EXTI input filtered pulse(expectedP20)	VDD=5.0V	5			us
T <sub>RST</sub>	NRST input filtered pulse	VDD=5.0V	10			us

## 6. 9. EFT Characteristics

Table 6- 10 EFT Characteristics

(TA=25°C, 5V)

Symbol	Parameters	Test Conditions	Pass Value	Unit
V <sub>EFT</sub>	Electrical Fast Transient	F <sub>sys</sub> =IHRC, BOR 关闭	±4500	V

## 6. 10. ESD Characteristics

Table 6- 11 ESD Characteristics

(TA=25°C, 5V)

Symbol	Parameters	Test Conditions	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage(human body model)	TA=25°C	±8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage(charge device model)		±2000	V

6.11. Latch up Characteristics

Table 6- 12 Latch up Characteristics

Symbol	Parameters	Test Conditions	Pass Value	Unit
LU	Latch up	TA=25°C,VDD=5V	±200	mA



**7. Chip type**

Chip type	Package	Pins
ATM8F8040A-KT3	TSSOP20	20
ATM8F8040A-KQ3	QFN20	20
ATM8F8040A-DS3	SOP16	16





## 8. Revision history

Rebision	Date	Changes
1.0	2024.06.20	Initial release

### **IMPORTANT NOTICE – PLEASE READ CAREFULLY**

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